WHAT IS CLAIMED IS:

1. An amplifier comprising:

a front amplification stage; and

a rear amplification stage which amplifies output signal of said front amplification stage, said rear amplification stage being disposed immediately after said front amplification stage, said rear amplification stage including a plurality of amplification unit connected in parallel, wherein amplification unit that forms a part of the plurality of amplification unit perform on/off switching of amplification operation according to an RF input of the front amplification stage or increase a bias current as the RF input increases.

2. An amplifier comprising:

a front stage transistor supplied with an RF signal;

an inter-stage matching circuit;

a rear stage transistor group having a plurality of transistors connected in parallel and supplied with an output signal of said front stage transistor via said inter-stage matching circuit; and

a rear stage DC bias control circuit which controls a bias of a transistor that forms a part of said rear stage transistor group according to an input level of the RF signal.

3. The amplifier according to claim 2, wherein said rear stage DC bias control circuit is connected between an emitter of said front stage transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit.

4. The amplifier according to claim 3, wherein said rear stage DC bias control circuit comprises AC blocking inductors connected in series between the emitter and the base, and a shunt resistor.

5. The amplifier according to claim 3, wherein said rear stage DC bias control circuit comprises an AC blocking inductor and a resistor connected in series between the emitter and the base, and a shunt resistor.

6. The amplifier according to claim 3, wherein said rear stage DC bias control circuit includes resistors connected in series between the emitter and the base, and a shunt resistor.

7. The amplifier according to claim 3, wherein said rear stage DC bias control circuit includes an AC blocking inductor and a resistor connected in series between the

emitter and the base, and a shunt diode.

8. The amplifier according to claim 3, wherein said rear stage DC bias control circuit includes resistors connected in series between the emitter and the base, and a shunt diode.

9. The amplifier according to claim 2, wherein said rear stage DC bias control circuit is connected between a source of said front stage transistor and a gate of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit.

10. The amplifier according to claim 9, wherein said rear stage DC bias control circuit includes AC blocking inductors connected in series between the source and the gate, and a shunt resistor.

11. The amplifier according to claim 9, wherein said rear stage DC bias control circuit includes an AC blocking inductor and a resistor connected in series between the source and the gate, and a shunt resistor.

12. The amplifier according to claim 9, wherein said rear stage DC bias control circuit includes resistors connected

in series between the source and the gate, and a shunt resistor.

13. The amplifier according to claim 9, wherein said rear stage DC bias control circuit includes an AC blocking inductor and a resistor connected in series between the source and the gate, and a shunt diode.

14. The amplifier according to claim 9, wherein said rear stage DC bias control circuit includes resistors connected in series between the source and the gate, and a shunt diode.

15. The amplifier according to claim 2, wherein said rear stage DC bias control circuit includes a control transistor supplied with the RF signal, and said control transistor controls a bias of a transistor that forms a part of said rear stage transistor group according to an input level of the RF signal.

16. The amplifier according to claim 15, wherein said front group transistor, a transistor included in the rear transistor group and supplied with a fixed bias, and said control transistor are biased so as to perform operation of class AB.

17. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes AC blocking inductors connected in series between an emitter of said control transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

18. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes an AC blocking inductor and a resistor connected in series between an emitter of said control transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

19. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes resistors connected in series between an emitter of said control transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

20. The amplifier according to claim 15, wherein said rear

stage DC bias control circuit further includes an AC blocking inductor and a resistor connected in series between an emitter of said control transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt diode.

21. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes resistors connected in series between an emitter of said control transistor and a base of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt diode.

22. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes AC blocking inductors connected in series between a source of said control transistor and a gate of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

23. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes an AC blocking inductor and a resistor connected in series between a source

of said control transistor and a gate of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

24. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes resistors connected in series between a source of said control transistor and a gate of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt resistor.

25. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes an AC blocking inductor and a resistor connected in series between a source of said control transistor and a gate of a transistor included in said rear stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt diode.

26. The amplifier according to claim 15, wherein said rear stage DC bias control circuit further includes resistors connected in series between a source of said control transistor and a gate of a transistor included in said rear

stage transistor group and supplied with a bias controlled by said rear stage DC bias control circuit, and a shunt diode.

27. The amplifier according to claim 2, wherein said front stage transistor, said inter-stage matching circuit, said rear stage transistor group, and the rear group DC bias control circuit are integrated on same semiconductor chip.

28. The amplifier according to claim 2, wherein said front stage transistor, said inter-stage matching circuit, said rear stage transistor group, and the rear group DC bias control circuit are provided distributively on two or more semiconductor chips.